

Interdata core memory. Low-cost, 2½ D organization.

Dual in-line integrated
circuit logic.

Expandable memory modules, 8 or 16
bit word length. Optional parity.



1.4 microseconds cycle time
800 nanoseconds access
and half cycle time.

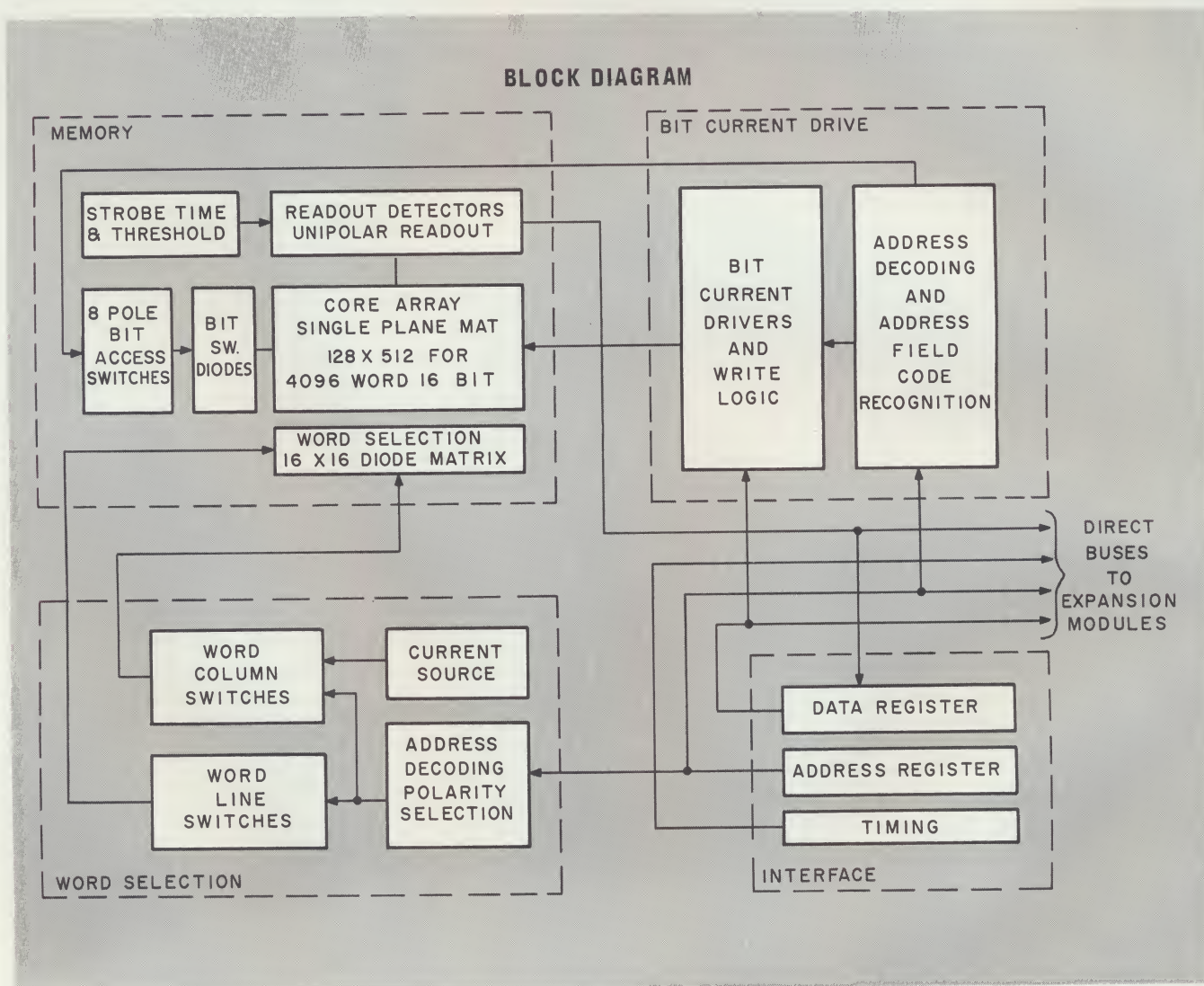
Unipolar readout with advanced
access switch design.

2 $\frac{1}{2}$ D CORE MEMORIES AT LESS THAN 10¢ A BIT

- LOW COST, HIGH PRODUCTION CORE MEMORY DESIGNED FOR THE INTERDATA MODEL 3 COMPUTER. AVAILABLE WITH OR WITHOUT INTERFACE LOGIC.
- LOW COST AT REASONABLE SPEED LESS THAN 10¢ A BIT FOR A USABLE MEMORY.
- LOGIC COMPONENTS ON MODULAR BOARDS FOR EASE OF MAINTENANCE WITH SMALL SPARE INVENTORY.
- HIGH RELIABILITY WITH FLAT MAT 2 $\frac{1}{2}$ D DESIGN MINIMIZING CONNECTION POINTS.

DESIGN FEATURES.

- COMPACT MULTIPOLE DIODE SWITCHES ON THE BIT ACCESS.
- UNIPOLAR CORE READOUT—USES LOW COST DETECTORS, SIMPLE LOGIC STROBE, AND A SINGLE THRESHOLD VOLTAGE AVAILABLE FOR MARGINAL TESTING
- INTERLACED WIRING PATTERN WITH ALTERNATE DRIVE POLARITY FOR CLEAN CURRENT PULSE TRANSMISSION THROUGH THE CORE ARRAY.
- PRINTED WIRE CONNECTIONS BETWEEN ACCESS DIODES AND CORE ARRAY.



FLEXIBLE SYSTEM CONNECTION

ELECTRICAL CHARACTERISTICS.

LOGIC SIGNAL LEVELS ARE STANDARD 830/930 SERIES DTL.

LOGICAL 0 0V. (NOM.) < 1.2V.
LOGICAL 1 5V. (NOM.) > 2.5V.

CONTROL SIGNALS.

BASIC MEMORY MODULES WITHOUT ADDRESS AND DATA REGISTERS OR TIMING.

Address Bus — 16 (12 OPTIONAL) BIT SINGLE RAIL.

Data Bus — 16 (OR 8) BIT SINGLE RAIL.

Data Answer — 16 (OR 8) BIT NEG GOING PULSE TO GROUND.

Timing — 6 LEADS (10 WITH PARITY) INCLUDING "SYSTEM CLEAR" THAT PROTECTS MEMORY DURING POWER ON/OFF. SEE TIMING DIAGRAM.

INTERFACE SIGNALS.

FOR INTERDATA STANDARD INTERFACE MODULES.

Input Address and Data — SINGLE RAIL, POSITIVE PULSE OR D.C.

Load Memory Address — CONTROL LEAD PULSE OR D.C.

Load Memory Data — CONTROL LEAD PULSE OR D.C.

System Clock — LEAD TO SYNCHRONIZE LOADING IF CONTROL IS D.C.

Data Output — BUFFERED REGISTER AND GATED PULSE.

Input Orders — "START" PULSE AND 2 BIT CODE. READ/ WRITE AND FULL/HALF CYCLE. (SEE TIMING DIAGRAM)

POWER REQUIREMENTS FOR 4096 WORD 16 BIT WITH PARITY

	MAX	IDLE
+5	2.0A.	1.5A.
+16 (NOM.)	2.0A.	1.0A.
-16 (NOM.)	1.0A.	

FOR FULL TEMPERATURE RANGE 0°C TO 50°C
±16V. TRACKS TEMPERATURE. ±17.5V AT 0°C
±15V. AT 50°C

MEMORY TIMING.

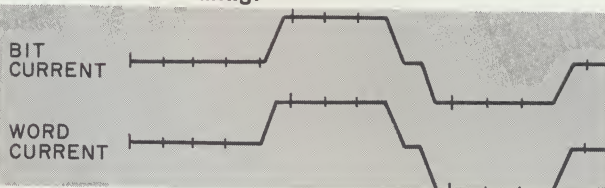
CYCLE TIME (MAX. FOR EXPANDED SYSTEMS)

• READ REGENERATE	RRG	1400 NSEC.
• ERASE AND WRITE	EAW	1400 NSEC.
• READ AND HALT	RAH	800 NSEC.
• WRITE AND HALT	WAH	700 NSEC.

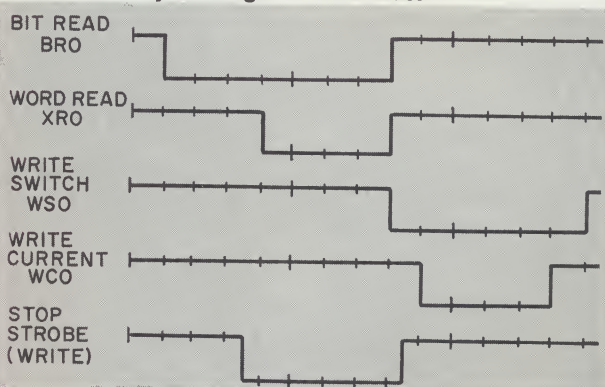
TIME NANOSECONDS



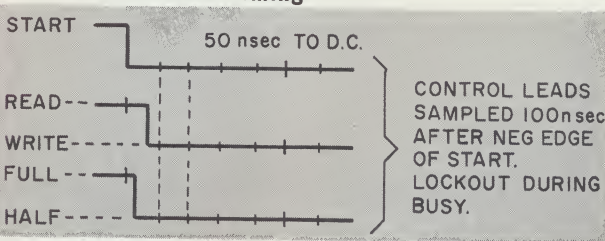
Drive Current Timing.



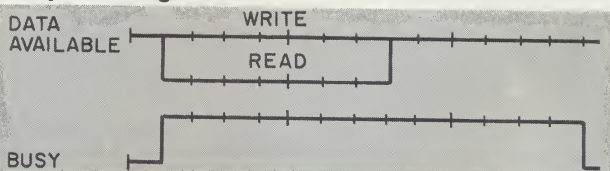
Basic Memory Timing (No Interface)



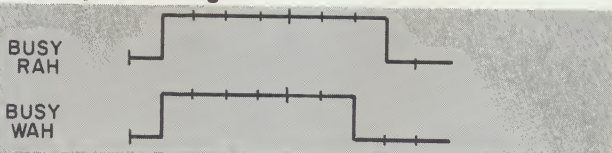
Standard Interface Timing



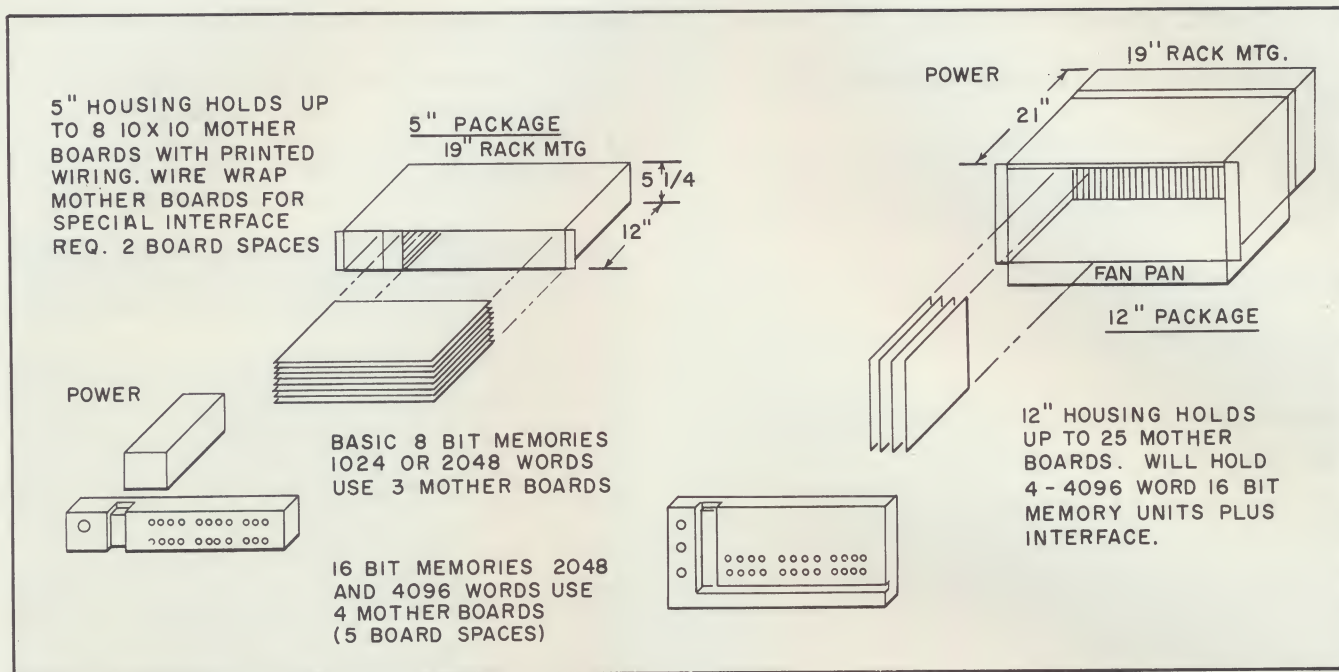
Output Timing



Half Cycle Timing.



FLEXIBLE MECHANICAL ARRANGEMENT



STANDARD SYSTEM CONFIGURATIONS				
MEMORY	INTERFACE	DISPLAY	POWER	CABINET
MEMORY MODULE 1024 WORD 8 BIT 3 BOARD POSITIONS	CUSTOM INTERFACE OR DO IT YOURSELF WIRE WRAP BOARD	5" COVER		5" RACK MOUNT
MEMORY MODULE 2048 WORD 8 BIT 3 BOARD POSITIONS	8 BIT INTERFACE ADDRESS & DATA REGISTER TIMING, PARITY OPT.	5" LAMP	5" POWER MODULE	5" CABINET
MEMORY MODULE 2048 WORD 16 BIT 5 BOARD POSITIONS	16 (8) BIT INTERFACE ADDRESS & DATA REGISTER TIMING	5" DISPLAY CLOCK & TEST		12" RACK MOUNT
MEMORY MODULE 4096 WORD 16 BIT 5 BOARD POSITIONS	16 BIT INCREMENTING ADDRESS REGISTER TEST CKTS.	12" COVER	10" POWER SUPPLY	12" CABINET
	16 BIT DATA REGISTER, TIMING, PARITY	12" DISPLAY CLOCK & TEST		
	DIRECT MEMORY ACCESS (DMA) PRIORITY & CONTROL			
	DMA CHANNEL			